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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/735,996

12/15/2003

G. Glenn Henry

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23669

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08/15/2006

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EXAMINER

FIEGLE, RYAN PAUL

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/735,996	<b>Applicant(s)</b> HENRY ET AL.	
	<b>Examiner</b> Ryan P. Fiegler	<b>Art Unit</b> 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 July 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 and 8-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 8-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

1. As noted by the applicant, the objections were not mandatory, and therefore they are withdrawn until allowable subject matter can be determined, as requested by the applicant.

### ***Claim Rejections - 35 USC § 112***

2. The examiner gratefully acknowledges and accepts the corrections to the claims to remedy the 112 issues.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6 and 8-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine et al. (US Patent 5,222,244) in view of the background of the specification.

5. As per claim 1:

A microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

a plurality of micro instruction queue entries, each corresponding to an instruction, and said each comprising a plurality of micro instructions and a microcode entry point (column 6, lines 58-68; column 7, lines 1-19); and

early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic (column 8, lines 39-46).

Carbine et al. do not teach the microprocessor apparatus comprising:

a translator, coupled to said plurality of micro instruction queue entries, configured to generate said microcode instruction queue entry (column 6, lines 58-68; column 7, lines 1-19).

Carbine does not disclose how the contents of the queue entries are determined.

However, the applicant has disclosed as prior art that the combination of a microcode ROM and a direct translator for the sequencing of macroinstructions is known in the art.

The combination of the microcode ROM and a direct translator in coordination with the microcode queue would be a viable, beneficial solution in Carbine.

An opposing possibility would be to statically populate the queue with the most commonly used instructions. One of ordinary skill in the pertinent art would have recognized that this would not be extremely useful because it would only provide the

benefits of not stalling on a microcode ROM instruction in the instance of encountering a common instruction, which might not extend across different applications.

In contrast, a queue that is dynamically populated by a translator when the microcode ROM instruction is first encountered will provide the benefits of the invention to all microcode ROM instructions.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that providing a translator to generate the microinstruction queue entries in Carbine would provide the benefit of not stalling on any microcode ROM instruction, rather than a select few.

6. As per claim 2:

The microprocessor apparatus as recited in claim 1, wherein said each of said plurality of micro instruction queue entries is provided in order to said register logic (column 6, lines 58-68; column 7, lines 1-19).

7. As per claim 3:

Carbine does not teach his queue containing four micro instruction queue entries; however, such would have been obvious to one of ordinary skill in the art.

Four entries provides a simpler design with a lower latency than designs with a greater number of entries. Further, less than four entries would not be beneficial because there would not be enough entries to make the additional logic beneficial.

In addition, it has been found that changing the size of an element does not designate a patentable difference if the invention would operate in the same manner. In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art that providing four entries in Carbine would provide the benefits of a simple logic and low latency while still providing the overall benefits of the invention.

8. As per claim 4:

The microprocessor apparatus as recited in claim 1, wherein said plurality of micro instructions comprises three micro instructions (column 7, lines 8-11).

9. As per claim 5:

The microprocessor apparatus as recited in claim 4, wherein the microcode ROM access delay comprises four clock cycles (It is inherent that the delay is 4 cycles since the queue contains the first three instructions).

10. As per claim 6:

The microprocessor apparatus as recited in claim 1, wherein said early access logic employs said microcode entry point when said microcode entry point is within a bottom micro instruction queue entry, said bottom micro instruction queue entry comprising one of said each, and wherein said bottom micro instruction queue entry will be provided to said register logic during a next clock cycle (column 6, lines 58-68; column 7, lines 1-19; column 8, lines 39-46).

11. As per claim 8:

The microprocessor apparatus as recited in claim 1, wherein said translator is configured to provide a generated micro instruction queue entry to a top micro instruction queue entry, wherein said top micro instruction queue entry comprises one of

said each micro instruction queue entry (This corresponds to the common FIFO definition of a queue).

12. As per claim 9:

The microprocessor apparatus as recited in claim 7, wherein said translator is configured to provide a generated micro instruction queue entry to a mux, and, when said plurality of micro instruction queue entries is empty, said mux provides said generated micro instruction queue entry to said register logic during a next clock cycle (It would have been obvious to one of ordinary skill in the pertinent art that if the queue is used in a FIFO manner where an entry is dequeued each cycle, an entry enqueued to an empty queue will take 5 cycles to reach the register logic which negates the purpose of the queue. Therefore, a bypass from the translator to the register logic would have been an obvious variation to one of ordinary skill in the pertinent art.).

13. As per claim 10:

The microprocessor apparatus as recited in claim 9, wherein said early access logic employs a bypass microcode entry point corresponding to said generated micro instruction queue entry (It is obvious that an entry point to the ROM will still need to be generated since the ROM will still need to be accessed after the first three instructions.).

14. As per claim 11:

An apparatus for absorbing pipeline stalls associated with microcode ROM access delay, the apparatus comprising:

a micro instruction queue, for providing a plurality of queue entries to register logic, each of said plurality of queue entries comprising:

first micro instructions, all of said first micro instructions corresponding to an instruction; and

a microcode entry point, coupled to said first micro instructions, configured to point to second micro instructions stored within a microcode ROM (column 6, lines 58-68; column 7, lines 1-19); and

early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access said microcode ROM prior to when said each of said plurality of queue entries is provided to said register logic, whereby a first one of said second micro instructions is provided to said register logic when said first one of said second micro instructions is required by said register logic (column 8, lines 39-46).

Carbine et al. do not teach the apparatus comprising:

a translator, coupled to said plurality of micro instruction queue entries, configured to generate said microcode instruction queue entry (column 6, lines 58-68; column 7, lines 1-19).

Carbine does not disclose how the contents of the queue entries are determined.

However, the applicant has disclosed as prior art that the combination of a microcode ROM and a direct translator for the sequencing of macroinstructions is known in the art.

The combination of the microcode ROM and a direct translator in coordination with the microcode queue would be a viable, beneficial solution in Carbine.

An opposing possibility would be to statically populate the queue with the most commonly used instructions. One of ordinary skill in the pertinent art would have



recognized that this would not be extremely useful because it would only provide the benefits of not stalling on a microcode ROM instruction in the instance of encountering a common instruction, which might not extend across different applications.

In contrast, a queue that is dynamically populated by a translator when the microcode ROM instruction is first encountered will provide the benefits of the invention to all microcode ROM instructions.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that providing a translator to generate the microinstruction queue entries in Carbine would provide the benefit of not stalling on any microcode ROM instruction, rather than a select few.

15. As per claims 12-16 and 18-20:

Claims 12-16 and 18-20 recite the same limitations as claims 1-6 and 8-10 and are rejected for the same reasons.

16. As per claim 17:

In the translation scheme presented in claim 11, the translator would generate each of the microinstruction queue entries.

17. As per claims 21-29:

Claims 21-29 recite the method of the apparatuses of claims 1-6, 17, 8 and 9, respectively, with the same limitations and therefore are rejected for the same reasons.

### ***Response to Arguments***

18. The applicant has made the following argument:

"First, the invention of Carbine does not teach a microinstruction queue, for receiving a plurality of queue entries from a translator, and for providing said plurality of queue entries to register logic. Carbine does not teach such a queue. Rather, Carbine teaches a translation ROM which is a large PLA which contains microinstructions. The microinstructions are the first two, or sometimes three microinstructions are part of a microcode flow that implements a particular complex instruction. This is substantially equivalent to Applicant's translator, but is in no way a queue of translated microinstructions, as is recited in claim 1."

The examiner disagrees with the applicant's assessment that Carbine's translation ROM is equivalent to the applicant's translator. The applicant's translator is a direct translation unit as addressed in paragraph 2 of section 48 of the applicant's disclosure. On the other hand, Carbine's translation ROM is a lookup translation unit.

A "queue" can be any number of things. While the term was typically used to refer to FIFO (first-in first-out) data structures in the past, it is used to define much broader data structures today. In a recent application examined by the examiner (10/334528), the applicant of that case defined queue as follows: "One skilled in the art will recognize that, as used herein, the term "queue" is used generally to refer to any manner of storing a group of related data." The examiner deemed this to be a satisfactory definition and has since then applied this definition to all instances of the word. Applied to Carbine, it is easy to see that the translation ROM is a queue since it stores sets of microinstructions and related data for macroinstructions.

The original version of the claims did not necessitate the queue entries to come from a translator, though the obviousness rejection made to claim 7 showed how Carbine would have the motivation to do so.

The translation ROM sends the microinstructions to the mousetrap multiplexer, which is the register logic. The mousetrap multiplexer, once it has all the translation

and aliasing data, forwards the microinstructions on the machine bus which accesses the register file (Figures 1 and 2).

19. The applicant has made the following argument:

"The translation ROM 122 which the Examiner points out in col. 8, lines 39-43, provides the first part of a microinstruction flow. Applicant's early access logic, in contrast, provides the second part of the micro instruction flow (from the microcode ROM) that corresponds to a complex instruction."

The citation of column 8, lines 39-43 was a typo. The citation meant to be made was column 8, lines 39-46. Specifically, lines 44-46 refer to an address forwarded by the translation ROM that says where the remainder of the instructions are fetched from the microcode ROM. The early access logic is a combination of the microflow word multiplexer logic and the unit which forwards the next fetch address for the microcode ROM from the translation ROM to the fetch unit (which holds the microcode ROM). This unit is not disclosed, but it is assumed to be logic contained in the mousetrap multiplexer. Nonetheless, it was not intended for the translation ROM to be interpreted as reading on the early access logic.

### ***Conclusion***

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegler whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegler

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Examiner  
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